IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:

George Apostol Jr. et al.

Application No.: 10/086,938

Filed: 02/28/2002

For: A MULTI-SERVICE SYSTEM-ON-A-CHIP INCLUDING ON-CHIP MEMORY WITH MULTIPLE ACCESS PATHS

Examiner: Knoll, Clifford H.

Art Unit: 2112

Confirmation No.: 3929

CERTIFICATE OF TRANSMISSION/MAILING

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AMENDMENT AND RESPONSE ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION

This communication is submitted in response to the Office Action mailed June 27, 2005 (hereinafter "Office Action") and the Applicant-Initiated Interview that took place on July 27, 2005 (hereinafter "Interview"). Reconsideration of the above captioned application in view of the amendments and remarks to follow is respectfully requested.

Summary of the Interview is found on page 2 of this paper.

Amendments to the claims are reflected in the listing of claims beginning on page 3 of this paper.

Remarks begin on page 10 of this paper.

SUMMARY OF THE INTERVIEW

The interview took place to clarify the use of Chen (U.S. Patent No. 5,197,130) (hereinafter "Chen") as a basis for various rejections in the Office Action. Claim 1 of the present application will be presented below with the Applicants' understanding of the Examiner's position as to which parts of Chen are relied upon for rejections in parenthesis:

an array of memory cells (memory portion **200** of Fig. 10);

a first data transfer interface coupled to the array of memory cells (X-ed block of Fig. 10 that provides access to the memory cells of Section 1 (hereinafter "X1")) to provide a first access path for a processor (Port **204** that provides access to X1 for the Arbitration node #16, of Fig. 3, over line **50** (hereinafter "Port $\mathbf{204_{1\text{-}16}}$")) and a subsystem of the IC (Port **204** that provides access to X1 for the MRCA **48** (Fig. 3) over line **54** (hereinafter "Port $\mathbf{204_{1\text{-}17}}$")) to access said array of memory cells;

a second data transfer interface coupled to the array of memory cells (X-ed block of Fig. 10 that provides access to the memory cells of Section 8 (hereinafter "X8")) to provide a second access path for said processor to access said array of memory cells ((Port **204** that provides access to X8 for the Arbitration node #16, of Fig. 3, over line **50** (hereinafter "Port $\mathbf{204_{8\text{-}16}}$"); and

a controller coupled to the array of memory cells and the first and second data transfer interfaces to control said array of memory cells and said first and second data transfer interfaces to facilitate accesses of said memory unit by said processor and said subsystem (various X-ed blocks and/or arbitration node **332** of Fig. 14).